Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X 60501

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Fourth Semester
Electrical and Electronics Engineering
EE 2255/EE 46/080280029/10133 EE 406 A – DIGITAL LOGIC CIRCUITS
(Regulations 2008/2010)
(Common to PTEE 2255 – Digital Logic Circuits for B.E. (Part-Time) Third Semester – EEE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Draw OR gate using NAND gates.

2. Give any two applications of decoders.

3. Draw the logic diagram of master slave D-Flip Flop using NAND gates.

4. Reduce the number of states in the following table and tabulate the reduced state table.

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

5. What is state assignment problem ?

6. What are the benefits of state reduction ?

7. What is Fan in and Fan out ? Give Fan in, Fan out characteristics of CMOS.

8. What ROM size is needed to implement a binary multiplier that multiplies two 4-bit numbers ?

9. What is the function of wait statement in VHDL package ?

10. Write the explanation of T'Base and T'Low predefined attributes.

PART – B **(5×16= 80 Marks)**

11. a) i) Express the function $F = A + \overline{B}C$ in
1) Canonical SOP form and
2) Canonical POS form. **(8)**

ii) Design BCD to Excess 3 code converter. **(8)**

(OR)

b) i) Simplify using K-map

F(A, B, C, D) = ∑m(7, 8, 9) + d(10, 11, 12, 13, 14, 15). **(8)**

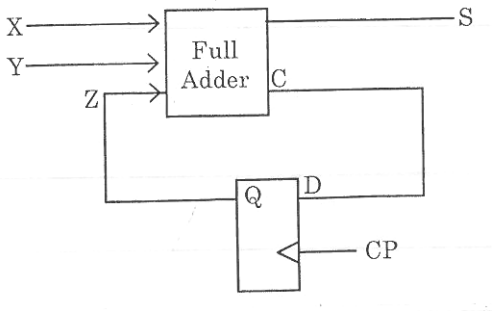
ii) Design a full subtractor using half subtractors. **(8)**

12. a) i) Design master-slave flipflop using RS flipflop. **(12)**

ii) Draw the logic diagram of clocked D flipflop with AND and NOR gates. **(4)**

(OR)

b) Obtain the state table and state diagram of the sequential circuit. **(16)**



13. a) i) Construct two input TTL NAND gate with three states output and explain its operation. Also discuss its merits and demerits. **(8)**

ii) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the complement of the input number. **(8)**

(OR)

b) i) A combinational circuit is defined by the functions : **(8)**

$F_1(A, B, C) = \sum(3, 5, 6, 7)$

$F_2(A, B, C) = \sum(0, 2, 4, 7)$

Implement the circuit with a PLA having three inputs, four product terms and two outputs.

ii) Derive the PLA programming table for the combinational circuit that squares a 3-bit number. Minimize the number of Product terms. **(8)**

14. a) i) How is memory modelled in VHDL ? Write a VHDL code that illustrates the read and write operations of memory. **(8)**

ii) Design and implement a 4-bit binary to Gray code converter using a PLA. **(8)**

(OR)

b) i) Compare the characteristics of TTL, ECL and CMOS logic families. **(6)**

ii) Design an AND-OR-PLA that implements the functions **(10)**

$f(x, y,z) = \Sigma m (0, 2, 4, 6)$

$g(x, y, z) = \Sigma m (1, 3, 5, 7)$.

15. a) Write HDL for four bit binary counter with parallel load and explain. **(16)**

(OR)

b) i) Write HDL for two to one line multiplexer with data flow description and behavioural description. **(8)**

ii) Write HDL for four bit adder. **(8)**

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